What is claimed is:

1. A method of generating a pattern for a semiconductor device comprising:

a layout pattern forming step of designing and arranging a layout pattern of a function element according to function information of a semiconductor chip;

a space area detecting step of detecting a space area in which no layout pattern exists;

a judging step of judging whether or not an MOS capacitor ell, the insulating film of which is a gate oxide film, can be arranged in the space area;

a step of arranging the MOS capacitor cell in the space judged that the MOS capacitor cell can be arranged; and

a wiring arrangement step of forming a wiring so that a gate conductor of the MOS capacitor cell can be connected to a first electric potential and a substrate can be connected to a second electric potential.

2. A method of generating a pattern for a semiconductor device according to claim 1, wherein the wiring arrangement step includes a step in which the gate conductor of the MOS capacitor cell is connected to a wiring of an electric power supply and a step in which the substrate is connected to a ground wiring.

3. A method of generating a pattern for a semiconductor device according to claim 2, wherein the wiring arrangement step includes a step in which a wiring layout pattern is generated so that a contact for connecting a wiring formed in an upper layer to the gate conductor can be formed and the wiring can be connected to the electric power supply wiring.

4. A method of generating a pattern for a semiconductor device according to claim 2, further comprising a step in which a wiring layout pattern is generated so that a contact of connecting the wiring formed in the upper layer to the substrate can be formed and the substrate can be connected to the ground wiring.

5. A method of generating a pattern for a semiconductor device according to claim 3, wherein the contact is connected to a contact formed in a portion, in which the electric power supply wiring or the ground wiring exists on a lower layer, via the wiring.

6. A method of generating a layout pattern for a semiconductor device according to claim 3, further comprising a step of extracting a region having no layout pattern of the function element and having no signal line above, wherein the wiring is arranged in the extracted

region.

7. A method of generating a layout pattern for a semiconductor device according to claim 6, the step of generating a layout pattern of the wiring comprising the step of:

detecting whether or not a front-end layer pattern exists from the layout pattern;

detecting whether or not a layout pattern of a function element exists on the same layer; and

extracting a region in which a wiring can be generated.

8. A method of generating a layout pattern for a semiconductor device according to claim 6, the step of generating a layout pattern of a wiring comprising the step of:

detecting whether or not a front-end pattern exists from the layout pattern and also detecting whether or not an upper layer pattern exists from the layout pattern;

detecting whether or not a layout pattern of a function element exists on the same layer; and

extracting a region in which an intermediate layer wiring, which is located between the front-end layer pattern and the upper layer pattern, can be generated.

9. A method of generating a pattern for a semiconductor device according to claim 1, wherein the wiring arrangement step is composed so that two continuous layers of dummy pattern cells have a cross like pattern and the dummy pattern cell of each layer has an island-shaped isolated pattern in a region corresponding to a cross region of the cross like pattern.

10. A method of generating a pattern for a semiconductor device according to claim 1, wherein the dummy pattern cell is composed of a first layer cell having a cross like pattern and an isolated island-shaped pattern in each of the four regions divided by the cross like pattern and also composed of a second layer cell, the pattern of which is a sharp-mark-shape arranged so that it crosses at four points corresponding to the island-shaped pattern, located on an upper layer or a lower layer continuing to the first layer cell, and the first layer and the second layer respectively compose an electric power supply wiring and a ground wiring.

11. A method of generating a pattern for a semiconductor device according to claim 1, further comprising:

a step of extracting an area ratio from the layout pattern of each layer composing the function element, the MOS capacitor element and the wiring; and

a dummy pattern adding step of adding a dummy pattern to the layout pattern so that the area ratio of the mask pattern of each layer can be adjusted to be the same while giving consideration to the most appropriate area ratio of the layout pattern for each layer obtained according to the process condition of each layer composing the layout pattern,

wherein the area ratio of each layer is adjusted to be the same.

12. A method of generating a semiconductor device according to claim 11, further comprising:

a step of dividing a layout pattern, which is formed in the layout pattern forming step, into small regions of a predetermined size;

a step of extracting an area ratio of the layout pattern for each small region divided; and

a dummy pattern adding step of adding a dummy pattern so that the area ratio of a mask pattern can be adjusted to be the same,

wherein the area ratio of each layer for each small region is adjusted to be the same.

13. A method of generating a pattern for a semiconductor device according to claim 12, further comprising:

a step of preparing a plurality of types of dummy pattern

cells, the area ratios of which are different from each other; and

the dummy pattern adding step including a step of selecting a predetermined dummy pattern cell according to the area ratio of the small region concerned.

14. A method of generating a pattern for a semiconductor device according to claim 12, further comprising a step in which an area ratio after the dummy pattern has been formed is calculated, it is judged whether or not the area ratio is in a predetermined range, when the area ratio is not in the predetermined range, some of the dummy patterns are replaced, and the most appropriate dummy cell is calculated.

15. A method of generating a pattern for a semiconductor device according to claim 11, wherein the dummy pattern adding step is executed for at least one of the wiring layer, the diffusing layer, the gate conductor and the well.

16. A device for generating a pattern used for a semiconductor device comprising:

a layout pattern forming means for forming a layout pattern from layout data of a semiconductor chip;

a space area detecting means for detecting a space area in which no layout pattern exists on the semiconductor chip;

a logic operation means for conducting a logic operation of a region detected by the space area detecting means and a design rule while consideration is given to technology by the design rule from the layout pattern formed by the layout pattern forming means; and

an arranging means for arranging a region extracted by the logic operation means so that it can be a decoupling capacitor adding arranging region.

17. A method of manufacturing a semiconductor device comprising:

a step of forming a mask pattern in each step according to the method described in claim 1,

and

a step of executing each process with the mask pattern so as to form a semiconductor device.

18. A semiconductor device comprising a pattern used for a semiconductor device generated by the method described in claim 1.

19 A semiconductor device according to claim 18 characterized in that: the semiconductor device is an aggregation composed of dummy capacitor cells of the same size; and the semiconductor device includes at least one dummy

capacitor cell not electrically connected.

21. A semiconductor device comprising a pattern used for a semiconductor device generated by the device described in claim 16.

20. A method of manufacturing a semiconductor device comprising:

a step of forming a mask pattern in each step according to the device described in claim 16;

and a step of executing each process with the mask pattern so as to form a semiconductor device.